

AMENDMENTS TO THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) A signal charge transfer line, which has been formed on a substrate and is formed to have a number of transfer electrodes, for transferring signal charge by application of transfer pulses to the transfer electrodes via electrode lines, wherein:
the number of transfer electrodes are divided into transfer electrodes of a plurality of sets to each of which a common transfer pulse is applied;
electrode lines for applying common transfer pulses to the transfer electrodes of the plurality of sets are formed on said substrate in common for each of the transfer electrodes of the plurality of sets; and
an output gate for outputting the signal charge transferred in the signal charge transfer line is formed on a final part of an output end of the signal charge transfer line; and
an ~~final~~ electrode line for applying a transfer pulse to a ~~final~~ transfer electrode at an
front of said output end gate is formed on said substrate independently of the electrode lines of respective ones of the plurality of sets.
2. (Currently Amended) The signal charge transfer line according to claim 1, further including a plurality of drivers provided in correspondence with respective ones of the plurality of sets of the transfer electrodes for applying transfer pulses to the corresponding sets of transfer electrodes;
wherein a transfer pulse applied by at least one driver among said plurality of drivers is applied to said ~~final~~ transfer electrode ~~via said final electrode line~~ in front of said output gate.
3. (Currently Amended) The signal charge transfer line according to claim 1, further including a synchronizing circuit for synchronizing transfer pulses applied to the transfer electrodes of the plurality of sets and the transfer pulse applied to said ~~final~~ transfer electrode in front of said output gate.

4. (New) The signal charge transfer line according to claim 1, wherein the transfer pulses, which are outputted from two inverting buffer circuits connected in series, are applied to the transfer electrodes of the plurality of sets, and wherein the transfer pulse, which is outputted from a non-inverting buffer circuit inputting a pulse is outputted from the first inverting buffer circuit of the two inverting buffer circuits.

5. (New) A signal charge transfer line, comprising:
a plurality of transfer electrodes, wherein a common transfer pulse is applied to each of the plurality of transfer electrodes;
a plurality of electrode lines for applying the common transfer pulse to each of the plurality of transfer electrodes; and
an output gate on an output end of the signal charge transfer line, wherein a separate electrode line is connected to a final transfer electrode independently of the plurality of electrode lines.

6. (New) The signal charge transfer line according to claim 5, wherein the final transfer electrode is located in between the plurality of transfer electrodes and the output gate.

7. (New) The signal charge transfer line according to claim 5, wherein the separate electrode line is connected only to the final transfer electrode.

8. (New) The signal charge transfer line according to claim 5, wherein the output gate is located on an output side of the final transfer electrode.

9. (New) The signal charge transfer line according to claim 5, wherein the separate electrode line applies a transfer pulse only to the final transfer electrode.

10. (New) The signal charge transfer line according to claim 5, wherein the separate electrode line applies a transfer pulse to the final transfer electrode independently from the common transfer pulse applied to each of the plurality of electrodes.

11. (New) A signal charge transfer line, comprising:
an electrode line means for applying a common transfer pulse to each or a plurality of transfer electrodes;
an output gate means for outputting a signal charge transferred in the signal charge transfer line; and
a separate electrode line means for applying a transfer pulse to a final transfer electrode,
wherein the separate electrode line means is independent of the electrode line means.
12. (New) The signal charge transfer line according to claim 5, wherein the final transfer electrode receives the transfer pulse only from the separate electrode line.
13. (New) The signal charge transfer line according to claim 11, wherein the final transfer electrode is located at an output end of the signal charge transfer line in between the plurality of transfer electrodes and the output gate means.
14. (New) The signal charge transfer line according to claim 11, wherein the separate electrode line means is connected only to the final transfer electrode.
15. (New) The signal charge transfer line according to claim 11, wherein the separate electrode line means applies a transfer pulse only to the final transfer electrode.
16. (New) The signal charge transfer line according to claim 11, wherein the output gate means is located at an output end of the signal charge transfer line.
17. (New) The signal charge transfer line according to claim 11, wherein the separate electrode line means applies a transfer pulse to the final transfer electrode independently from the common transfer pulse applied to each of the plurality of electrodes.
18. (New) The signal charge transfer line according to claim 11, wherein the final transfer electrode receives the transfer pulse only from the separate electrode line means.

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19. (New) The signal charge transfer line according to claim 1, wherein the electrode line is connected only to the transfer electrode in front of said output gate.
20. (New) The signal charge transfer line according to claim 1, wherein the electrode line applies a transfer pulse only to the transfer electrode in front of said output gate.